Silicon Gate MOS 8308

8192 BIT STATIC MOS READ ONLY MEMORY
Organization -- 1024 Words x 8 Bits

- Fast Access – 450 ns
- Directly Compatible with 8080 CPU at Maximum Processor Speed
- Two Chip Select Inputs for Easy Memory Expansion
- Directly TTL Compatible – All Inputs and Outputs
- Three State Output – OR-Tie Capability
- Fully Decoded
- Standard Power Supplies +12V DC, ±5V DC

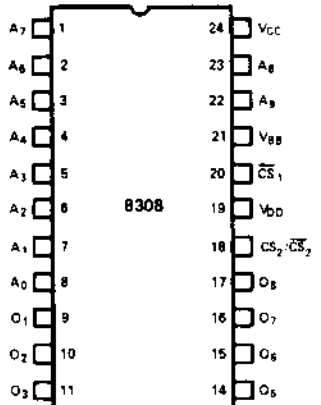
The Intel® 8308 is an 8,192 bit static MOS mask programmable Read Only Memory organized as 1024 words by 8-bits. This ROM is designed for 8080 microcomputer system applications where high performance, large bit storage, and simple interfacing are important design objectives. The inputs and outputs are fully TTL compatible.

A pin for pin compatible electrically programmed erasable ROM, the Intel® 8708, is available for system development and small quantity production use.

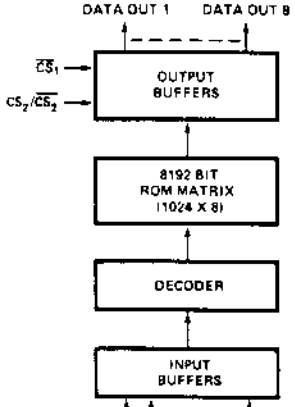
Two Chip Selects are provided – $\overline{CS}_1$ which is negative true, and $CS_2/\overline{CS}_2$ which may be programmed either negative or positive true at the mask level.

The 8308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}_1$, CS_2	CHIP SELECT INPUTS

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To V_{BB} . . . . . -0.3V to 20V
Power Dissipation . . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

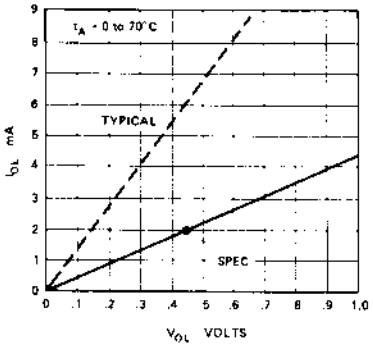
D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

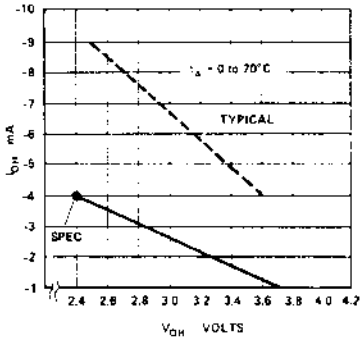
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS}_1$)			10	µA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS}_1$			1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS}_1$			4	mA	V_{IN} = 0.8V to 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS}_1$			10	µA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	µA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}-1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = -4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = -1mA
I_{CC}	Power Supply Current V_{CC}		.8	2	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		10µA	1	mA	
P_D	Power Dissipation			775	mW	

NOTE 1: Typical values for T_A = 25°C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS



D.C. OUTPUT CHARACTERISTICS



A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]			Unit
		Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay Time		200	450	ns
t_{CO_1}	Chip Select 1 to Output Delay Time		85	160	ns
t_{CO_2}	Chip Select 2 to Output Delay Time		125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time		125	220	ns

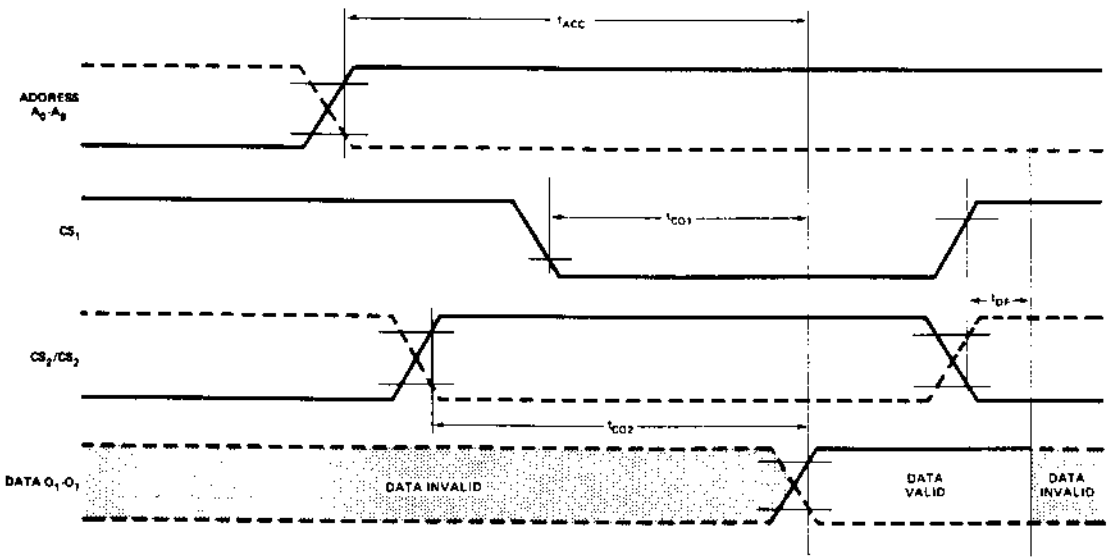
NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at V_{OH} = 3.7V @ I_{OH} = −1mA, C_L = 100pF.

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate, and C_{LOAD} = 100pF
Input Pulse Levels . . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . . 20 nsec
Timing Measurement Reference Level
. . . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

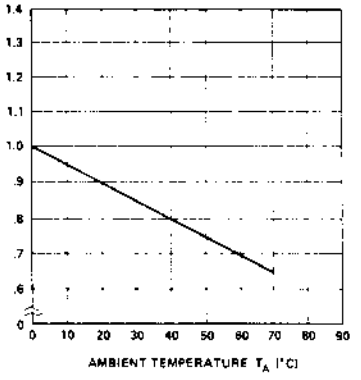
CAPACITANCE T_A = 25°C, f = 1 MHz, V_{BB} = −5V, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF

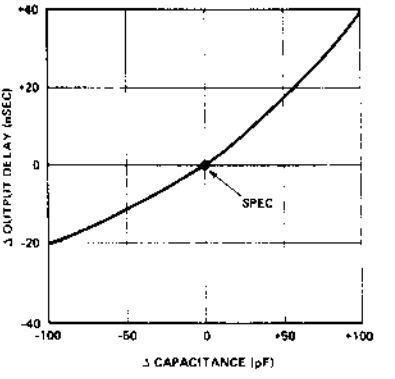


Typical Characteristics (Nominal supply voltages unless otherwise noted.)

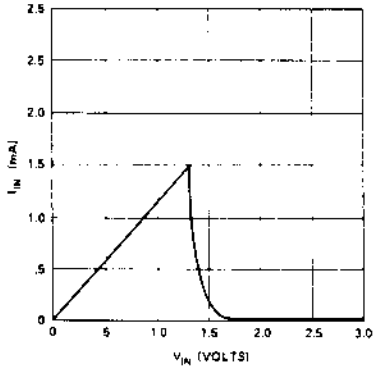
I_{DD} VS. TEMPERATURE (NORMALIZED)



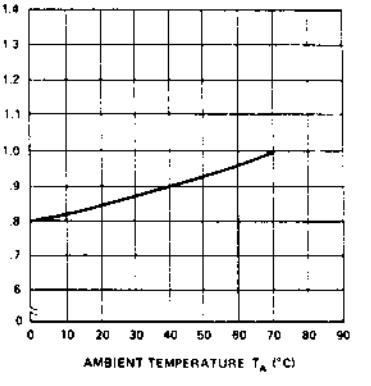
Δ OUTPUT CAPACITANCE VS. Δ OUTPUT DELAY



$\overline{CS_1}$ INPUT CHARACTERISTICS



T_{ACC} VS. TEMPERATURE (NORMALIZED)



MCS™ CUSTOM ROM ORDER FORM

8308 ROM

CUSTOMER _____

P.O. NUMBER _____

DATE _____

For Intel use only

S# _____ PPPP _____

STD _____ ZZ _____

_____ DD _____

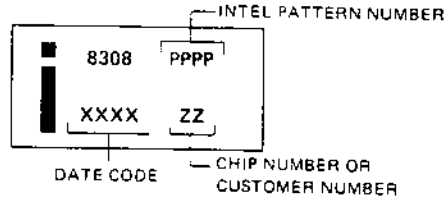
APP _____ DATE _____

All custom 8308 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P8308), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 9 characters or spaces).

CUSTOMER NUMBER _____



MASK OPTION SPECIFICATIONS

A. CHIP NUMBER (CHIP SELECT OPTION)

Must be specified 0 or 1.

The chip number will be coded in terms of positive logic where a logic "1" is high level input.

Chip Select Truth Table

Chip Number	$\overline{CS1}$	CS2	Selected
0	0	0	Yes
1	0	1	Yes
0	1	0	No
1	1	1	No

Chip Number _____

B. ROM Truth Table Format

Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table should be accompanied with the order.

The following general format is applicable to the programming information sent to Intel:

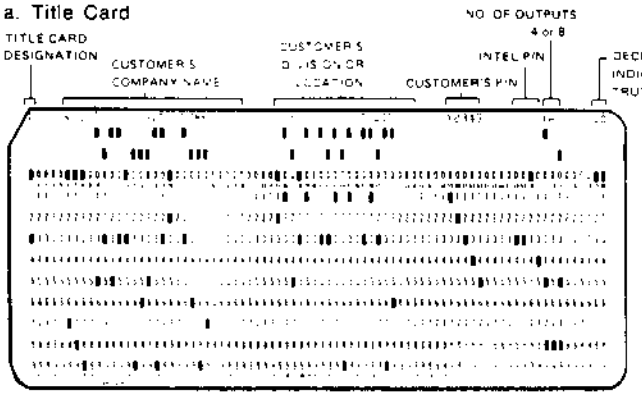
- Data fields should be ordered beginning with the least significant address (0000) and ending with the most significant address (1023).
- A data field should start with the most significant bit and end with the least significant bit.
- The data field should consist of P's and N's. A P is to indicate a high level output (most positive) and an N a low level output (most negative). In terms of positive logic, a P is defined as a logic "1" and an N is defined as a logic "0". If the programming information is sent on a punched paper tape, then a start character, B, and an end character, F, must be used in the data field. See paragraph 2.

1. Punched Card Format

An 80-column Hollerith card (preferably interpreted) punched by an IBM 026 or 029 keypunch should be submitted. The first card will be a title card; the format is as follows:

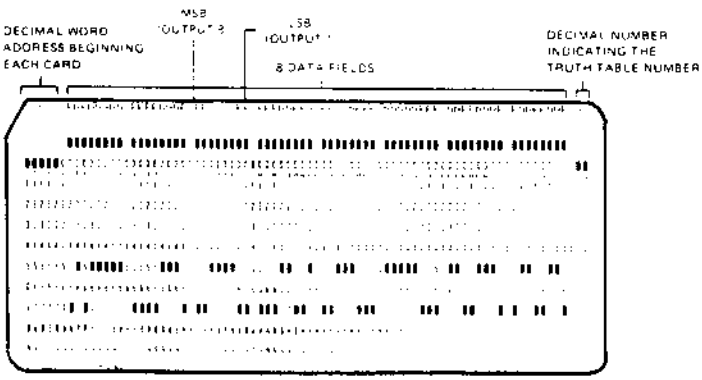
MCS™ CUSTOM ROM ORDER FORM 8308

a. Title Card



Column	Data
1	Punch a T
2–5	Blank
6–30	Customer Company Name
31–34	Blank
35–54	Customer's Company Division or location
55–57	Blank
58–66	Customer Part Number
67	Blank
68–75	Punch the Intel 4-digit basic part number and in ( ) the number of output bits e.g., 8308(8).
76–78	Blank
79–80	Punch a 2-digit decimal number to identify the truth table number (mask programmed chip select number).

b. For a 1024 word X 8-bit organization only, cards 2 and the following cards should be punched as shown.



Column	Data
1–5	Punch the 5-digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., 00000, 00008, 00016 etc.
6	Blank
7–14	Data Field
15	Blank
16–23	Data Field
33	Blank
34–41	Data Field
42	Blank
43–50	Data Field
51	Blank
52–59	Data Field
60	Blank
61–68	Data Field
69	Blank
70–77	Data Field
78	Blank
79–80	Punch same 2-digit decimal number as in title card.

2. Paper Tape Format

1" wide paper tape using 7- or 8-bit ASCII code, such as a model 33 ASR teletype produces, or the 11/16" wide paper tape using a 5-bit Baudot code, such as a Telex produces.

The format requirements are as follows:

a. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly 1024 word fields for the 1024 X 8 ROM organization.

b. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F.

NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape an error is made, the entire word field, including the B and F, must be rubbed out. Within the word field, a P results in a high level output and an N results in a low level output.

c. Preceding the first word field and following the last word field, there must be a leader/trailer length of *at least 25 characters. This should consist of rubout or null punches (letter key for Telex tapes).*

d. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.

e. Included in the tape before the leader should be the customer's complete Telex or TWX number and, if more than one pattern is being transmitted, the ROM pattern number.

f. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.